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Citation	M. S. Baig and A. I. Hussein, "Cognitive Radio Receiver Design Employing Pipeline Successive Approximation ADC," 2025 22nd International Learning and Technology Conference (L&T), jeddah, Saudi Arabia, 2025, pp. 136-141, doi: 10.1109/LT64002.2025.10940955.
Download date	2026-06-13 21:56:19
Link to Item	https://repository.effatuniversity.edu.sa/handle/20.500.14131/2104

Cognitive Radio Receiver Design Employing Pipeline Successive Approximation ADC

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2025 22nd International Learning and Technology Conference (L&T) | 979-8-3315-3221-5/25/$31.00 ©2025 IEEE | DOI: 10.1109/LT64002.2025.10940955

Abstract— **Smart cities require better cellular communication, incorporating a high data rate that satisfies the Internet, cloud computing, and the Internet of Things (IoT) requirements. A high data rate demands higher bandwidth with low latency. However, the already saturated or underutilized frequency spectrum hinders this realization. 5G and cognitive radio technology can enhance spectrum utilization to meet the high data demands of future cellular communication. Cognitive radio uses spectrum sensing to identify underutilized frequencies without interfering with licensed users, addressing the scarcity of the electromagnetic spectrum. In this paper, a cognitive radio receiver design with a SAR analog-to-digital converter, which is recognized for having a modest resolution for high bandwidth signals, is implemented. Moreover, the pipeline technique in the SAR design is proposed to increase the resolution to be suitable for 5G applications. The high-level model of the system is simulated using MATLAB Simulink software. The quantization error observed in the regular SAR ADC design is compared to that in the proposed pipeline SAR ADC, highlighting the enhanced accuracy and efficiency of the pipeline SAR ADC, which makes it suitable for spectrum sensing in next-generation cognitive radio systems.**

Keywords: Smart cities, 5G, Cognitive Radio, Spectrum Sensing, Pipeline SAR ADC

I. INTRODUCTION

A smart city is defined as the culmination of the Internet, cloud computing, the Internet of Things (IoT), and other new information technologies combined with traditional cities. To realize the concept of Smart cities, apart from several other factors also, it is necessary to implement IoT and 5G networks as a necessary technology for this implementation. Hence, there is an inherent connection between 5G and smart cities. Figure 1 represents how 5G can be used in managing smart cities [1].

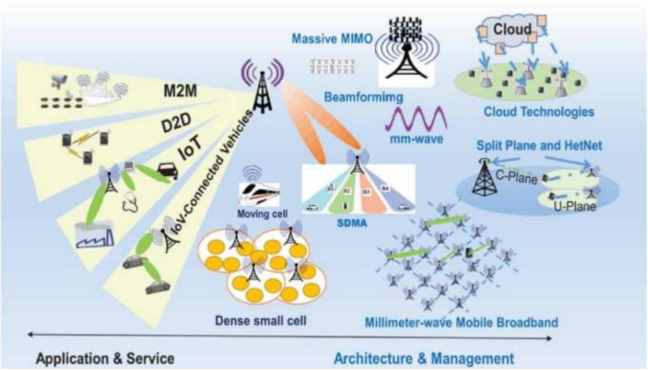

Fig. 1. 5G's applications and features [1].

The purpose of 5G technology is to provide larger bandwidth, low latency, and low power consumption. 5G technology will work in tandem with Cognitive Radio to meet the high data load of future cellular communication.

The electromagnetic spectrum is a scarce resource strictly controlled and licensed by governments. Unfortunately, fixed spectrum allocation leads to underutilization when a dedicated spectrum is inactive. According to studies done by the USA Federal Communications Commission (FCC) [2], the conventional fixed spectrum allocation rules have led to low spectrum usage efficiency in almost all currently deployed frequency bands. 5G technology seeks to resolve this issue using Cognitive radio through spectrum sensing [3][4][5][6][7].

Mitola and Maguire [8] offered cognitive radio to address spectrum shortages in next-generation cellular networks using time, frequency, and space domains. Cognitive radio would detect RF signals in its environment and automatically modify its operational settings to network infrastructure while matching user expectations.

To achieve the above stated goal the cognitive radio is made of two parts: (1) a hardware unit, and (2) an intelligence unit, which supplies the radio with the necessary software-based intelligence.

Like any other communication device, the hardware unit of Cognitive radio contains a transmitter and a receiver. However, unlike a standard wireless transceiver, a cognitive radio must transmit and receive signals and monitor the spectrum in real-time, referred to as spectrum sensing.

Spectrum sensing captures a snapshot for a broad range of frequencies, which aids the cognitive radio in identifying unused frequencies and protocols to employ and begins signaling at that frequency.

Cognitive radio must optimally utilize underutilized spectrum, also known as spectral opportunities, as shown in Figure 2, without interfering with primary users (PUs), as they are considered secondary users using PUs licensed frequency. Furthermore, PUs are not required to exchange or adjust their operational settings while sharing spectrum with cognitive radio networks. Therefore, without the assistance of PUs, cognitive radios should be able to identify spectral possibilities; this capacity is called spectrum sensing, and it is considered to be one of the key elements of cognitive radio networks [3][5][9].

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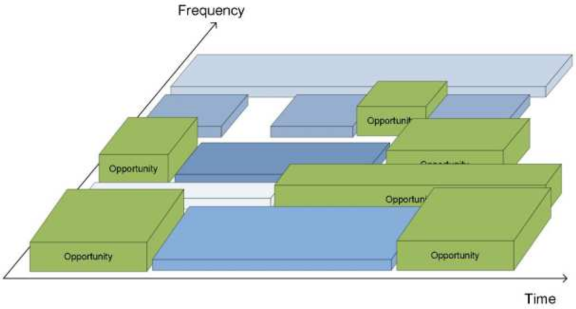

Fig. 2. Spectral opportunities [10].

Spectrum sensing is divided into Narrowband and Wideband methods, with techniques in each category assessed for advantages and disadvantages .With the growing need for high data transmission rates in modern communication systems, bandwidth requirements have increased. This forces cognitive radios (CRs) to scan large sections of the spectrum, at high frequencies, to identify available channels before transmission. To meet this need, different wideband spectrum sensing techniques have been introduced [3][11][12].

Figure 3 provides an overview of these methods by category [3][9][13].

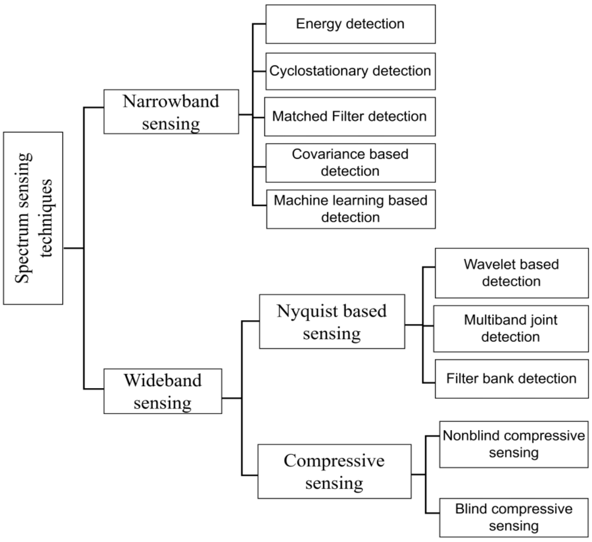

Fig. 3. Types of spectrum sensing [14].

II. RELATED WORK

In [1], the authors showed that 5G, with its high speed, low latency, and large capacity, is ideal for supporting smart cities and enabling efficient technologies like autonomous driving, smart healthcare, and energy management. Furthermore, the authors articulate that 5G meets the demand for reliable and fast connectivity, which is crucial for meeting the needs of smart city infrastructures and shaping future urban living.

With 5G deployment underway globally, offering low latency and high connectivity, future demands are driving research toward 6G cognitive radio (CR) networks. Aiming for global coverage, enhanced efficiency, and AI integration, 6G will support ultra-high data rates and advanced security, facilitating smart applications through a seamless mix of terrestrial and satellite networks [15].

According to the authors of [3], cognitive radio networks (CRNs) increase spectrum efficiency by giving secondary users access to licensed spectrum that isn't being used. Spectrum sensing is critical for detecting the status of the spectrum, with traditional methods like energy detection being simple but ineffective at low SNR. Modern techniques use statistical information and machine learning to improve performance, though selecting optimal features remains challenging. The paper also highlights the need for further research into spectrum sensing for 5G CRNs.

The authors of [4] go over a number of spectrum sensing strategies, such as robust approaches, matched filtering, cyclostationary detection, energy detection, likelihood ratio testing, eigenvalue-based sensing, and matched filtering. Additionally, cooperative sensing with several receivers is investigated. Techniques that need less previous knowledge of the source signal and propagation channel are emphasized. Test statistic distributions and threshold choices are theoretically analyzed, and the difficulties of noise power uncertainty are discussed.

Several studies have investigated different Analog-to-Digital Converters (ADC) as a key component in the cognitive radio transceiver. Those studies include but are not limited to, Sigma-Delta, Successive Approximation Register (SAR), Pipeline, and Flash ADCs, each having various advantages and trade-offs, as mentioned in [16], [17], and [18].

In [19], the authors presented a 12-bit SAR ADC architecture using a hybrid RC DAC and digital calibration to improve conversion accuracy while reducing circuit space. The ADC employed a combined digital-analog method, including digital calibration to ensure accuracy within 2 LSB at high clock speeds. This design displayed effective accuracy and efficient power consumption, which aligns well with low-power, high-precision application requirements.

In order to lower power consumption in situations with low input signal activity, including biological signals, the authors of [20] describe a modified SAR ADC architecture and switching approach. By extracting only, the least significant bits of slow-varying samples, their approach consumed less power in both the DAC and comparator.

With a 1.8 V supply, 180 nm CMOS technology, a passive sample-and-hold circuit, and a capacitor-based DAC, another research demonstrated a SAR ADC with an SNDR of 52.1 dB and a power usage of just 53 µW [21].

In [22], the authors developed a SAR ADC for biomedical uses that can be integrated into sensor systems. To address the low-power and accuracy requirements of biomedical applications, the researchers designed the ADC using 90nm CMOS technology at 1.2V using Synopsys EDA tools.

The authors in [23] describe an 8-bit Asynchronous SAR ADC made using modern 18nm FinFET technology. It includes an internal clock generator, a bootstrapped sample-and-hold circuit, a dynamic comparator, a precision DAC, and SAR logic. The ADC has ultra-low power consumption in the microwatt range, making it ideal for applications requiring efficient power consumption, moderate resolution, and fast speed, such as biomedical sensors and AI-driven memory cores.

In [24], a capacitive array DAC architecture was developed in the second stage to lower the OTA's power consumption, and aggressive gain reduction was used in the residual amplifier. The number of bits in each ADC pipeline stage were determined by an in-depth power consumption analysis.

This paper presents a pipeline SAR ADC design and analysis for a cognitive radio receiver for a 5G cellular system. ADC is an essential component in cognitive radio, especially for spectrum sensing, where accurate and efficient signal conversion is required. We aim to compare the performance outcomes of a standard SAR ADC with those of the Pipeline SAR ADC, focusing on quantization error. Through this comparison, we aim to highlight the advantages of the Pipeline SAR ADC.

III. PROPOSED RECEIVER DESIGN

The hardware of the CR receiver is depicted in Figure 4. A digital end and a radio frequency (RF) front end make up the receiver. The front end of RF is made up of a low noise amplifier(LNA), variable voltage gain(VGA), and automatic gain controller(AGC). The Digital end comprises an analog-to-digital converter (ADC), digital down converter DDC, and baseband processing block, including spectrum sensing.

When an RF signal is first received, it is down-converted to a baseband signal by the RF front-end block. The signal is then provided to ADC for digital samples to DDC [25]. As discussed in the introduction, spectrum sensing is a fundamental component in CR; this operation is done in the baseband processing block of the CR receiver using one of the spectrum sensing techniques shown in Figure 3.

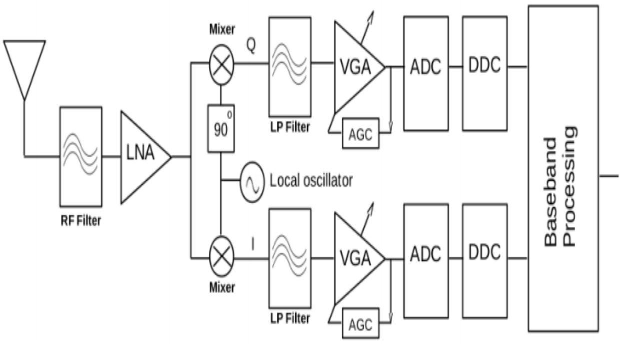

Fig. 4. CR receiver architecture—wideband radio [25].

Effective spectrum sensing in cognitive radio applications requires ADCs with high sampling rates, significant resolution, broad dynamic range, and efficient high-speed signal processing capabilities [10].

As seen in Figure 4, an ADC is therefore one of the most important components in the design of cognitive radio hardware; its function is to transform analogue signals into digital formats for digital processing, storage, and transmission.

In General, ADCs can be divided into four widely used types, as shown in Figure 5[26].

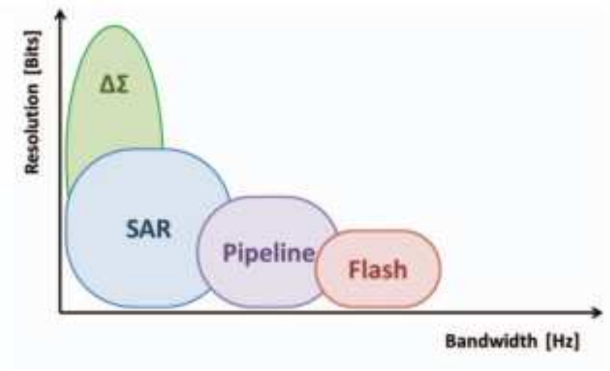

Fig. 5. Resolution versus Bandwidth for different ADCs

The Figure depicts the behavior of resolution versus bandwidths for different ADCs. Flash ADCs can be used for high speed and low resolution, however when it comes to high-resolution requirements, Σ-Δ ADCs are a better choice. Conventional Pipeline ADCs, which offer High resolution and High sampling speeds have been improved to provide greater efficiency by implementing SAR design.

As shown in Figure 6, the SAR-assisted pipeline ADC is a two-stage pipeline with SAR architecture to implement both stages of the ADC design. This design offers linearity and reduced amplifier power requirements by providing high resolution in the first stage of its architecture. Compared to SAR ADC, the design has high throughput and relaxed comparator noise [26].

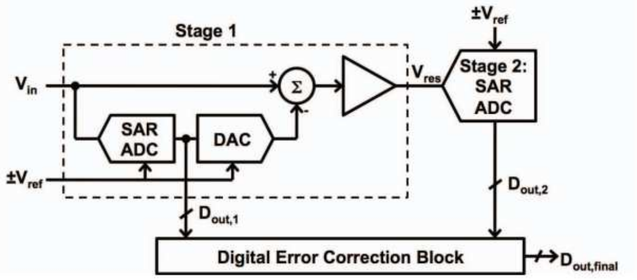

Fig. 6. Pipeline SAR ADC

This study emphasizes the design of a 12-bit SAR assisted Pipeline ADC, utilizing MATLAB for implementation.

IV. SIMULATION & RESULTS

A comparator, a digital-to-analog converter (DAC), a sequential approximation register (SAR), and a Sample/Hold (S/H) circuit make up each step of the SAR-assisted pipeline ADC, as seen in Figure 7[27].

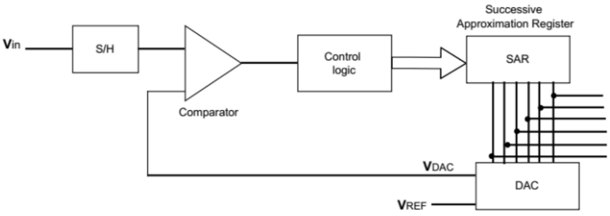

Fig. 7. Block Diagram of SAR ADC

A sine wave input was generated with a defined amplitude and frequency(1MHz), allowing for a comprehensive analysis of the ADC's performance. The DAC's reference voltage (Vref) was adjusted to 3.3V, allowing the ADC to operate within its maximum range. A Sample-and-Hold block was used to acquire the instantaneous voltage of the input signal, with a sample duration of 20nsec to assure precise timing during conversion. Relational operator was used to compare the DAC output with the held analogue voltage. The DAC's digital output was changed in response to comparisons performed throughout the successive approximation process, allowing the SAR to efficiently converge to the proper digital value. MATLAB functions were used to simulate both the DAC and the SAR logic, simplifying computation and enabling real-time examination of the conversion process.

The SAR (Successive Approximation Register) block employed a binary search algorithm. In this method each bit of the digital output is found by sequentially comparing the input signal to a reference voltage that is adjusted based on prior bit selections. This algorithm allows the SAR ADC to quickly converge to the closest digital representation of the input voltage, making it efficient for converting analog signals with high resolution.

In order to verify the fundamental block diagram of the SAR ADC the model was designed in Simulink, as shown in Figure 8, for a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) .

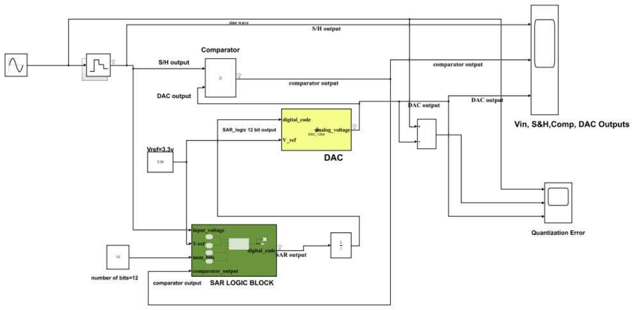

Fig. 8. Simulink Model

As previously stated, a sine wave with a frequency of 1Mhz was provided as input and sampled at 20MHz using a Sample and Hold simulation block. Figure 9 depicts both the input wave and its sampled version.

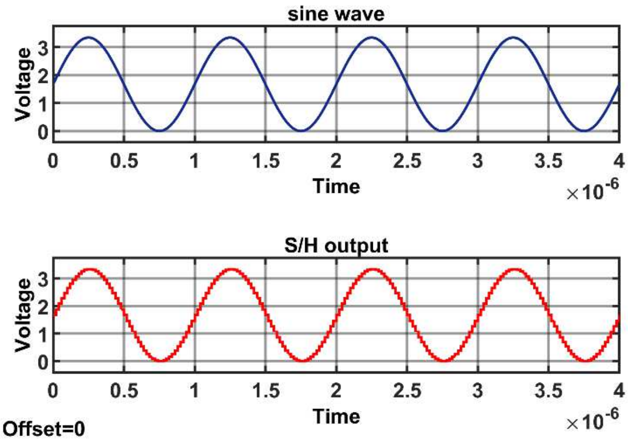

Fig. 9. Sine wave & S/H Output

The output from the comparator, which was designed using a relationship operator in Simulink, and DAC are shown in Figure 10. The comparator remains high during the time analog sampled version of Vin>VDAC and shifts to zero when Vin<VDAC. From the waveform obtained it can be seen that the comparator performance was good. The waveforms are stacked together to show the transition of S/H, comparator and Vdac output over time.

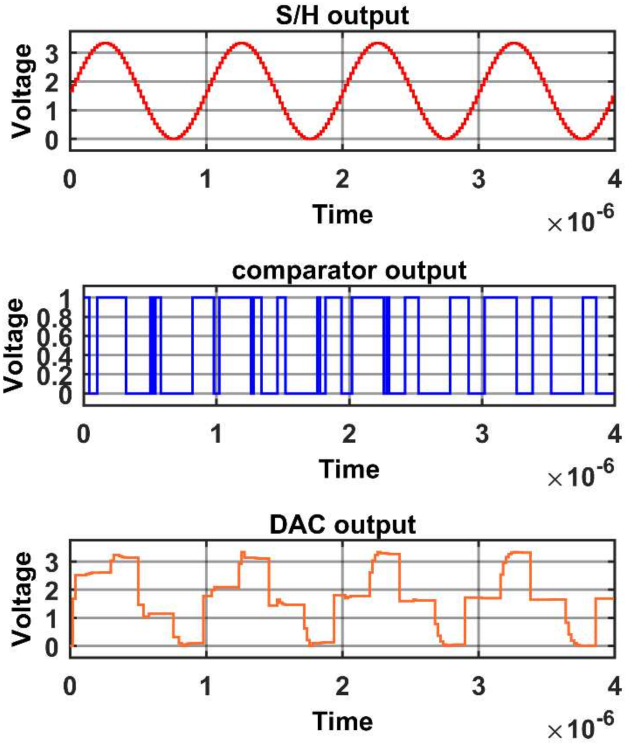

Fig. 10. Illustration of Vdac, comparator & sample & Hold Output

Setting up timing control is critical to guarantee that the SAR ADC operation runs in synchronization with the comparison and bit correction processes. The Timing diagram for SAR logic block SAR logic which already manages bit timing correctly and steps through each bit as intended using the binary search algorithm, is shown in Figure 12. The SAR logic block generates 12-bit binary code and the output of DAC changes in accordance with the binary code received.

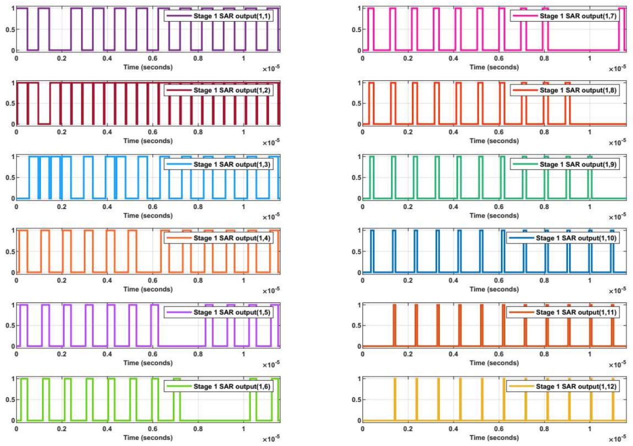

Fig. 11. SAR Logic Timing waveform

Figure 12 shows the error, also referred to as quantization error, between analog sine wave input the DAC output.

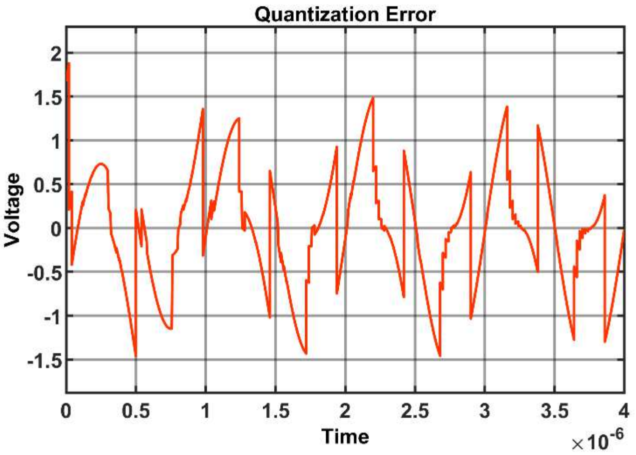

Fig. 12. Quantization Error

The mean square error (MSE) for the above quantization error was found to be 0.4348.

Based on the fundamental design of SAR ADC, a two stage Pipeline SAR ADC was designed as shown in Figure 13.

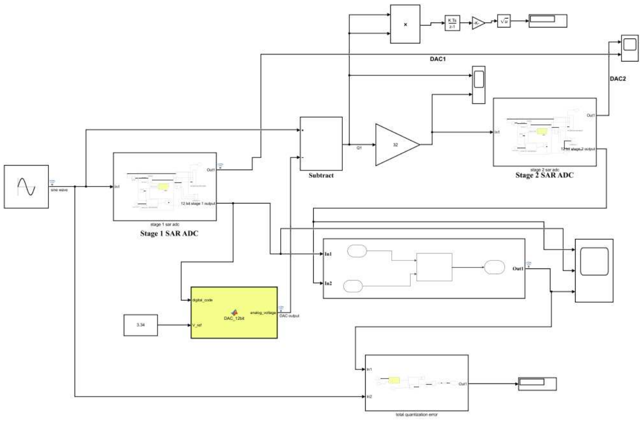

Fig. 13. Simulink Model for Pipeline SAR ADC

The gain for residue amplifier was chosen such that it gave minimum quantization error. Figure 14 shows the output from the first stage of pipeline SAR ADC and 15 show the outputs from each DAC of stage 2 of pipeline SAR ADC.

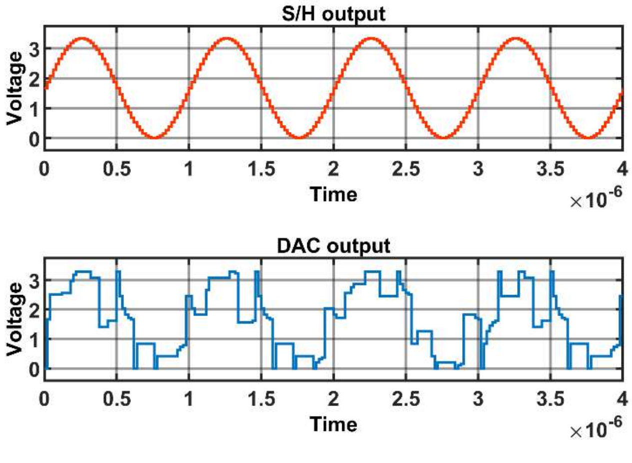

Fig. 14. Stage 1 Sample /Hold versus DAC output

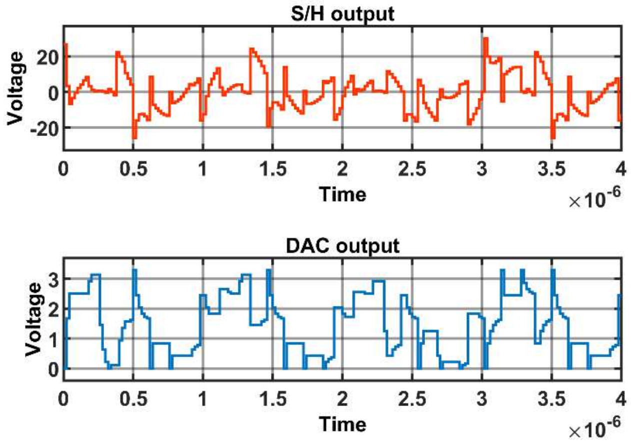

Fig. 15. Stage 2 Sample /Hold versus DAC output

Figure 15 shows the reconstructed analog signal from the combined digital output ($D_{out,Final}$), as was shown in Figure 6, from stage1 SAR ADC and stage2 SAR ADC. It can be observed that this reconstructed output signal is a better approximation of the input signal as compared to the reconstructed signal using a simple SAR ADC.

V. CONCLUSION

In this paper, a cognitive radio receiver design with a SAR analog-to-digital converter, which is known for its modest resolution for high bandwidth signals, is implemented. Moreover, the pipelining approach is employed to enhance this traditional SAR's performance. MATLAB Simulink software is used that simulates the system's high-level model. The quantization error observed in the regular SAR ADC design is compared to that in the proposed pipeline SAR ADC, highlighting the enhanced accuracy and efficiency of the pipeline SAR ADC, which makes it suitable for spectrum sensing in next-generation cognitive radio systems.

REFERENCES

[1] Zhuang, Feiyang. "5G mobile communication systems application in smart cities." Applied and Computational Engineering 12 (2023): 108-114.

[2] Force, S. "Spectrum policy task force report." Federal Communications Commission ET Docket 02, vol. 135 (2002).

[3] Muzaffar, Muhammad Umair, and Rula Sharqi. "A review of spectrum sensing in modern cognitive radio networks." Telecommunication Systems 85.2 (2024): 347-363.

[4] Zeng, Yonghong, et al. "A review on spectrum sensing for cognitive radio: challenges and solutions." EURASIP journal on advances in signal processing 2010 (2010): 1-15.

[5] Sasipriya, S., and R. Vigneshram. "An overview of cognitive radio in 5G wireless communications." 2016 IEEE international conference on computational intelligence and computing research (ICCIC). IEEE, 2016.

[6] Zeng, Yonghong, and Ying-Chang Liang. "Spectrum-sensing algorithms for cognitive radio based on statistical covariances." IEEE transactions on Vehicular Technology 58.4 (2008): 1804-1815.

[7] Ghasemi, Amir, and Elvino S. Sousa. "Spectrum sensing in cognitive radio networks: requirements, challenges and design trade-offs." IEEE Communications magazine 46.4 (2008): 32-39.

[8] Mitola, Joseph, and Gerald Q. Maguire. "Cognitive radio: making software radios more personal." IEEE personal communications 6.4 (1999): 13-18.

[9] Sun, Hongjian, et al. "Wideband spectrum sensing for cognitive radio networks: a survey." IEEE Wireless Communications 20.2 (2013): 74-81.

[10] Yucek, Tevfik, and Huseyin Arslan. "A survey of spectrum sensing algorithms for cognitive radio applications." IEEE communications surveys & tutorials 11.1 (2009): 116-130.

[11] Sadhu, Bodhisatwa, and Ramesh Harjani. Cognitive radio receiver front-ends: RF/analog circuit techniques. Vol. 115. Springer Science & Business Media, 2013.

[12] Hwang, Chien-Hwa, Guan-Long Lai, and Shih-Chang Chen. "Spectrum sensing in wideband OFDM cognitive radios." IEEE Transactions on Signal Processing 58.2 (2009): 709-719.

[13] M. Mourad Mabrook, Hussein A. Taha & Aziza I. Hussein. Cooperative spectrum sensing optimization based adaptive neuro-fuzzy inference system (ANFIS) in cognitive radio networks. J Ambient Intell Human Comput, Springer (2020).

[14] Arjoune, Youness, and Naima Kaabouch. "A comprehensive survey on spectrum sensing in cognitive radio networks: Recent advances, new challenges, and future research directions." Sensors 19.1 (2019): 126.

[15] Aslam, Muhammad Muzamil, et al. "Sixth generation (6G) cognitive radio network (CRN) application, requirements, security issues, and key challenges." Wireless Communications and Mobile Computing 2021.1 (2021): 1331428.

[16] Thin, Mon Mon, Myo Min Than, and Theingi Myint. Enhancement of SAR algorithm for analog to digital converter. Diss. MERAL Portal, 2015.

[17] Jamuna, S., P. Dinesha, and K. P. Shashikala. "A brief review on types and design methods of ADC." J. Eng. Res. Appl. 8.6 (2018): 85-91.

[18] Verma, Aakanksha, and B. S. Saini. "Comparative Analysis and Review of ADCs and Comparators for Use in Biomedical Applications." 2024 2nd International Conference on Computer, Communication and Control (IC4). IEEE, 2024.

[19] Wang, Deming, et al. "Design of a 12-Bit SAR ADC with Calibration Technology." Electronics 13.3 (2024): 548.

[20] Sepehrian, Hassan, Mehdi Saberi, and Reza Lotfi. "A signal-specific successive-approximation analog-to-digital converter." 2011 IEEE International Symposium of Circuits and Systems (ISCAS). IEEE, 2011.

[21] Pilipko, Mikhail M., and Mikhail E. Manokhin. "Design of a Low-Power 12-bit SAR ADC." 2019 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus). IEEE, 2019.

[22] Carandang, Jomar, et al. "Development of a low power 8-bit successive approximation register ADC in 90nm process technology for biomedical application." TENCON 2017-2017 IEEE Region 10 Conference. IEEE, 2017.

[23] Kalaiselvi, A., et al. "Design and Analysis of SAR-ADC for Low Power Circuits." 2024 IEEE International Conference on Information Technology, Electronics and Intelligent Communication Systems (ICITEICS). IEEE, 2024.

[24] Chen, Kairang, Prakash Harikumar, and Atila Alvandpour. "Design of a 12.8 ENOB, 1 kS/s pipelined SAR ADC in 0.35-μm CMOS." Analog Integrated Circuits and Signal Processing 86 (2016): 87-98.

[25] THAMEUR, HAYFA BEN. "Spectrum Sensing Using Software Defined Radio for Cognitive Radio Networks: A Survey."

[26] Fredenburg, Jeffrey, and Michael P. Flynn. "ADC trends and impact on SAR ADC architecture and analysis." 2015 IEEE Custom Integrated Circuits Conference (CICC). IEEE, 2015.

[27] Kolte, Durgesh, and Tejas Khandale. "A Review on Successive Approximation ADC." International Research Journal of Engineering and Technology 8.8 (2021): 1668-1674.